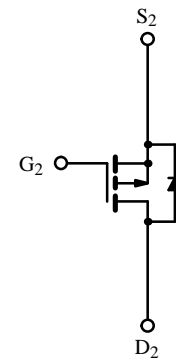
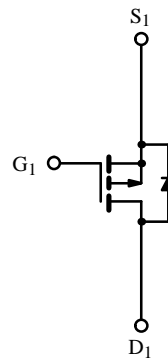
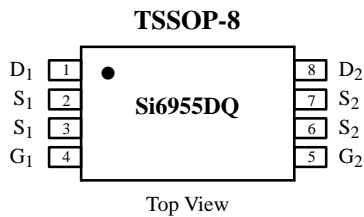


Dual P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.085 @ $V_{GS} = -10$ V	± 2.5
	0.19 @ $V_{GS} = -4.5$ V	± 1.8



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	A
		$T_A = 70^\circ\text{C}$	
Pulsed Drain Current	I_{DM}	± 20	
Continuous Source Current (Diode Conduction) ^a	I_S	-1.25	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	W
		$T_A = 70^\circ\text{C}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	125	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Subsequent updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1813.

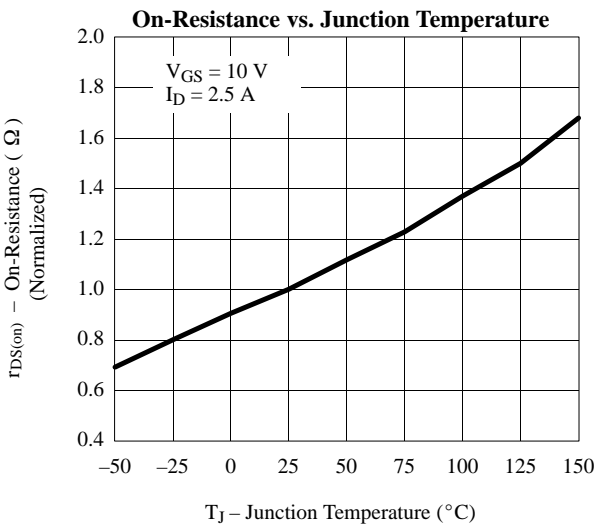
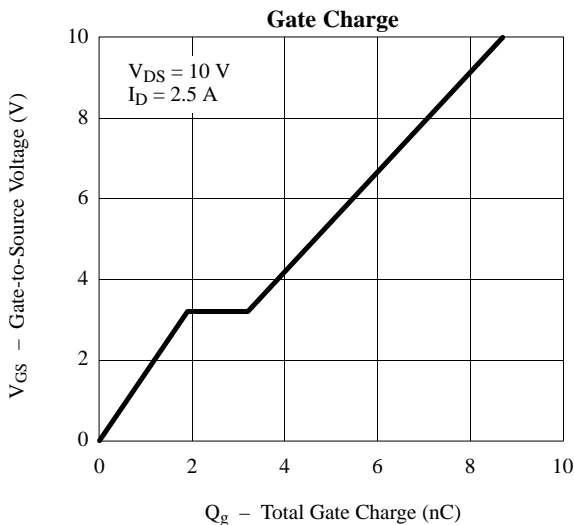
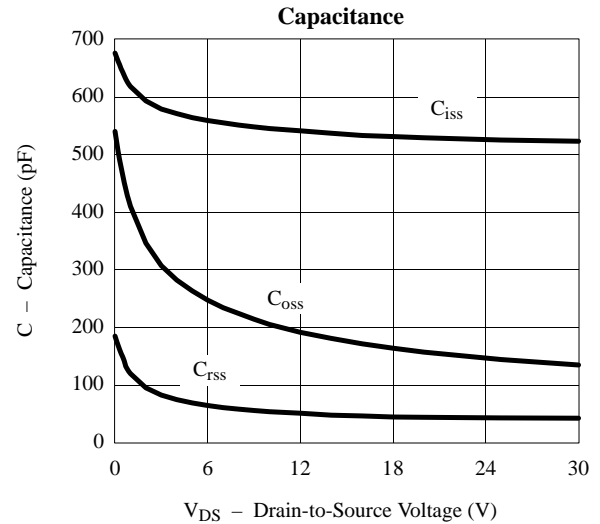
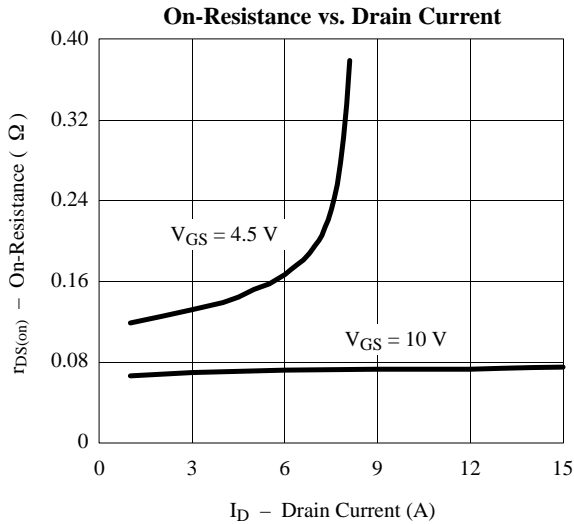
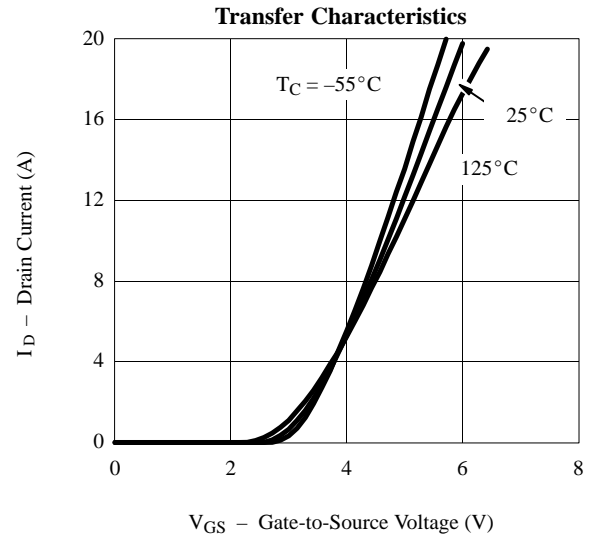
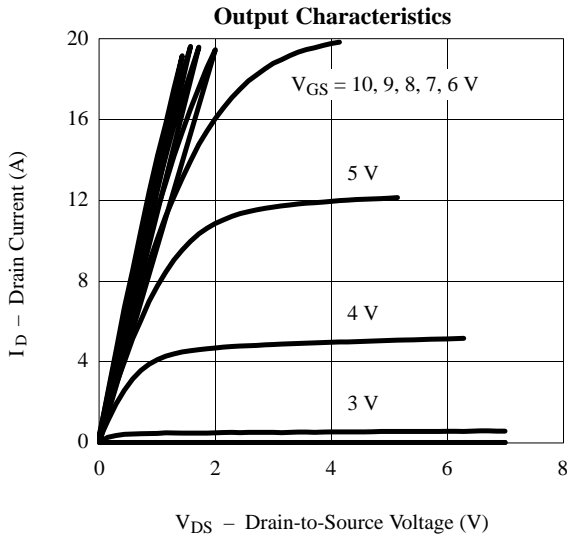
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	1.0			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μA
		$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq -5 \text{ V}, V_{GS} = -10 \text{ V}$	-15			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10 \text{ V}, I_D = 2.5 \text{ A}$		0.066	0.085	Ω
		$V_{GS} = -4.5 \text{ V}, I_D = 1.8 \text{ A}$		0.125	0.19	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15 \text{ V}, I_D = -2.5 \text{ A}$		5		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.25 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -10 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -2.5 \text{ A}$		8.7	15	nC
Gate-Source Charge	Q_{gs}			1.9		
Gate-Drain Charge	Q_{gd}			1.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10 \text{ V}, R_L = 10 \Omega$ $I_D \cong -1 \text{ A}, V_{GEN} = -10 \text{ V}, R_G = 6 \Omega$		7	15	ns
Rise Time	t_r			9	18	
Turn-Off Delay Time	$t_{d(off)}$			14	27	
Fall Time	t_f			8	15	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.25 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		46	80	

Notes

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Otherwise Noted)



Typical Characteristics (25°C Unless Otherwise Noted)

